Project Plan

Team: sddec23-08

Problem Statement

Ideal:

- Iowa State University would have access to fabricated ReRAM chips for research purposes
- Iowa State University would have institutional knowledge of how the analog design flow works for the Skywater 130nm process

Reality:

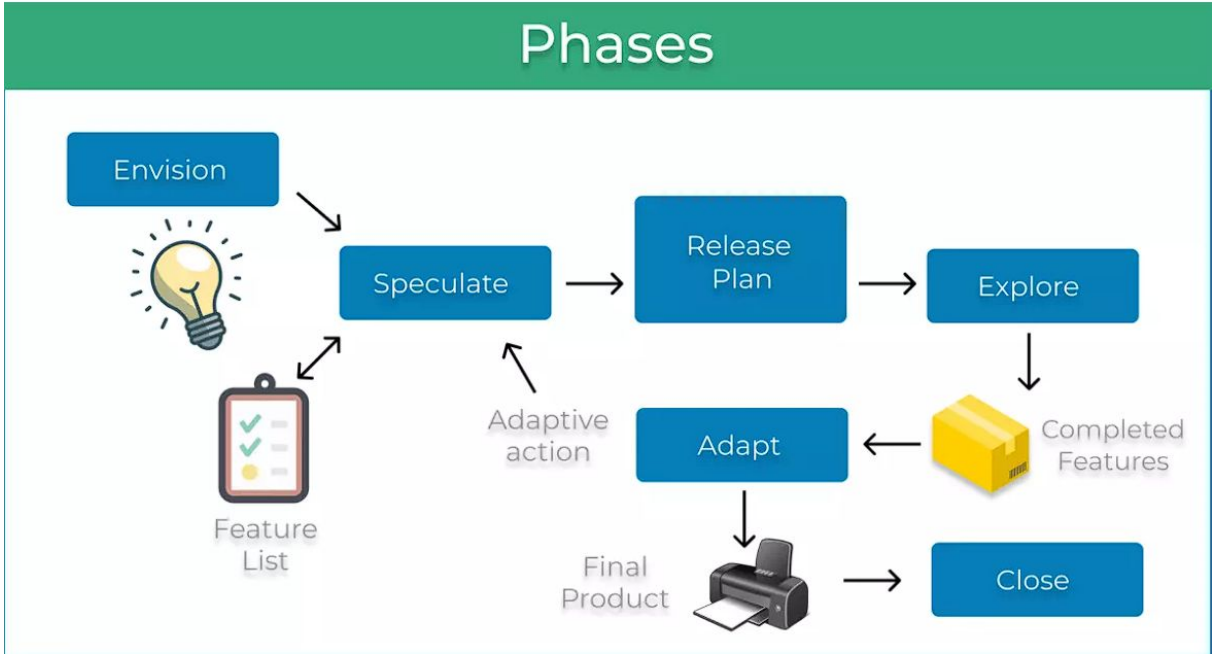
- It is difficult to get any fabricated chip, especially one with ReRAM, because of how new of a technology it is.
- Iowa State University has never produced a fabricated analog chip on the Skywater 130nm processed

Proposal:

- Use eFabless's MPW shuttle program to submit a ReRAM chip proposal.
    - If it gets approved, it would give us access to fabricated ReRAM chips
    - Along the way, we would document our workflow, contributing the ISU's internal knowledge of analog fabrication in the Skywater 130nm process.

Project Management Style

- Our team will employ the agile management style
- This project will require continuous testing and iteration
- The Agile management style will allows us to receive feedback and implement it quickly



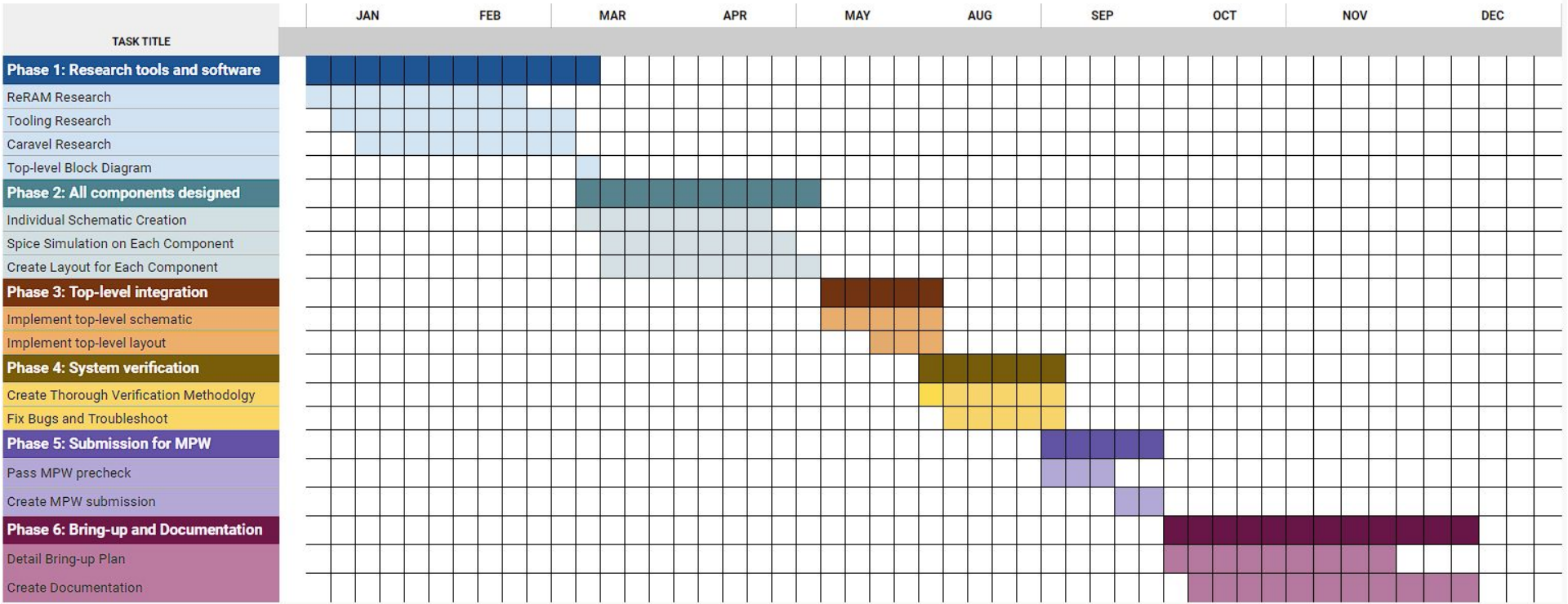
Task Decomposition

- Research will be done by all members
- Analog component creation will be split up between Joshua, Matthew, and Regassa
- Digital components will be created by Aiden
- Top-level integration and testing with Caravel harness will be worked on by all members
- Everyone will contribute to documentation and bring-up plan

TASK TITLE
Phase 1: Research tools and software
ReRAM Research
Tooling Research
Caravel Research
Top-level Block Diagram
Phase 2: All components designed
Individual Schematic Creation
Spice Simulation on Each Component
Create Layout for Each Component
Phase 3: Top-level integration
Implement top-level schematic
Implement top-level layout
Phase 4: System verification
Create Thorough Verification Methodolgy
Fix Bugs and Troubleshoot
Phase 5: Submission for MPW
Pass MPW precheck
Create MPW submission
Phase 6: Bring-up and Documentation
Detail Bring-up Plan
Create Documentation

Project Schedule

ReRAM Crossbar ASIC Fabrication



Risks/Risk Mitigation

- There is a very slight risk the the Efabless program might end before we can submit
  - We have no control over this
- Minor risk comes up from not completing design of all components in time for submission or design not passing precheck
  - We can mitigate this by staying on top of our schedule
- Major risk comes from the top-level design not achieving the desired functionality
  - We can mitigate this by thoroughly testing all components, and using proper troubleshooting strategies

Possible Risk	Probability
Efabless program gets suspended	3%
Unable to implement all components in time	10%
Top-level fuctionaility is not desirable	25%
Design not able to pass precheck	10%

Personal Effort Level

- Project will roughly take about 200 total hours from research to submission to bring-up plan
- This work will be spread out between team members
- Different team members will be contributing more than others depending on what phase of the project we are in

TASK TITLE	Effort
Phase 1: Research tools and software	**63 hr**
ReRAM Research	20 hr
Tooling Research	20 hr
Caravel Research	20 hr
Top-level Block Diagram	3 hr
Phase 2: All components designed	**Variable**
Individual Schematic Creation	2 hr / component
Spice Simulation on Each Component	15 hr / component
Create Layout for Each Component	5 hr / component
Phase 3: Top-level integration	**40 hr**
Implement top-level schematic	20 hr
Implement top-level layout	20 hr
Phase 4: System verification	**40 hr**
Create Thorough Verification Methodolgy	20 hr
Fix Bugs and Troubleshoot	20 hr
Phase 5: Submission for MPW	**11 hr**
Pass MPW precheck	10 hr
Create MPW submission	1 hr
Phase 6: Bring-up and Documentation	**45 hr**
Detail Bring-up Plan	30 hr
Create Documentation	15 hr